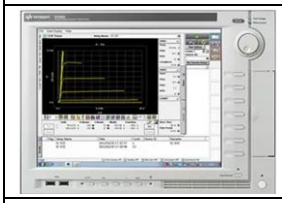
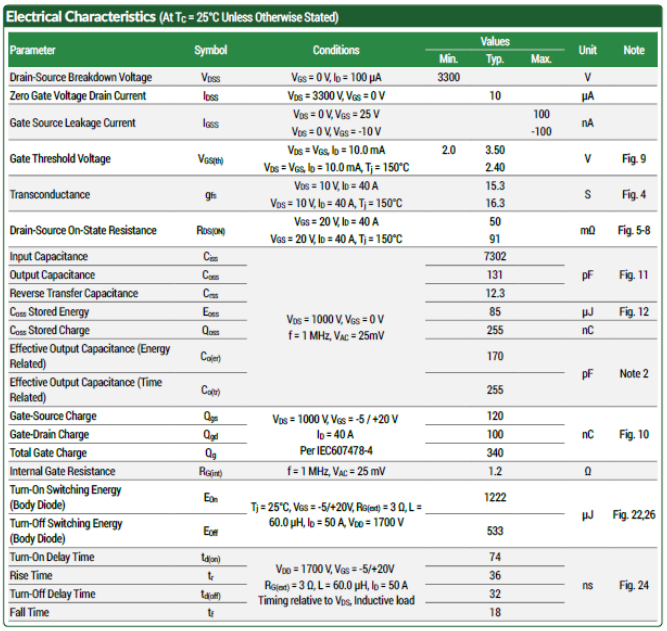
POMME One Bottom Datasheet

TF-WBG-OBDS software datasheet

Keysight

B1505A	B1506A
	
PD1500A	PD1550A
	

Datasheet



Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	3300			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 3300 V, V_{GS} = 0 V		10		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 25 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10.0 mA V_{DS} = V_{GS}, I_D = 10.0 mA, T_j = 150°C	2.0	3.50 2.40		V	Fig. 9
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 40 A V_{DS} = 10 V, I_D = 40 A, T_j = 150°C		15.3 16.3		S	Fig. 4
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 20 V, I_D = 40 A V_{GS} = 20 V, I_D = 40 A, T_j = 150°C		50 91		mΩ	Fig. 5-8
Input Capacitance	C_{iss}	V_{DS} = 1000 V, V_{GS} = 0 V f = 1 MHz, V_{AC} = 25mV		7302		pF	Fig. 11
Output Capacitance	C_{oss}			131			
Reverse Transfer Capacitance	C_{rss}			12.3			
C_{oss} Stored Energy	E_{oss}			85		µJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			255		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			170		pF	Note 2
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			255			
Gate-Source Charge	Q_{gs}	V_{DS} = 1000 V, V_{GS} = -5 / +20 V I_D = 40 A Per IEC607478-4		120		nC	Fig. 10
Gate-Drain Charge	Q_{gd}			100			
Total Gate Charge	Q_g			340			
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		1.2		Ω	
Turn-On Switching Energy (Body Diode)	E_{on}	T_j = 25°C, V_{GS} = -5/+20V, $R_{G(ext)}$ = 3 Ω, L = 60.0 µH, I_D = 50 A, V_{DD} = 1700 V		1222		µJ	Fig. 22,26
Turn-Off Switching Energy (Body Diode)	E_{off}			533			
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1700 V, V_{GS} = -5/+20V $R_{G(ext)}$ = 3 Ω, L = 60.0 µH, I_D = 50 A Timing relative to V_{DS}, Inductive load		74		ns	Fig. 24
Rise Time	t_r			36			
Turn-Off Delay Time	$t_{d(off)}$			32			
Fall Time	t_f			18			

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

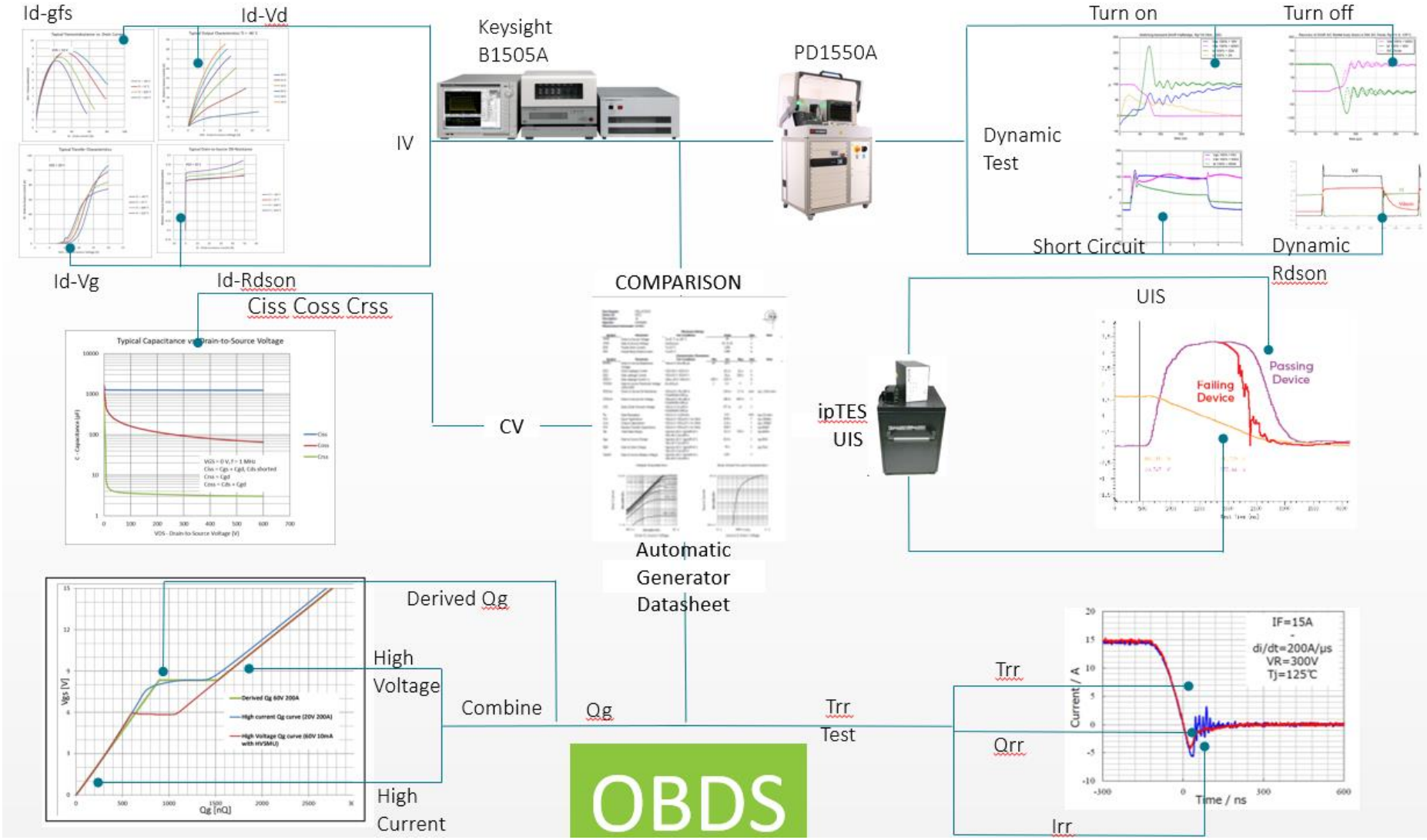
Note 2: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 1000V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 1000V.

Datasheet Generate

1. Application

- Ducking to static Keysight B1505A and B1506A.
- Ducking to dynamic Keysight PD1500A and PD1550A.
- Ducking to ipTEST DC/AC testing station.
- Easy transfer from DC/AC characterization equipment raw data to datasheet.

2. Software figure



3. Available Test Item

	Power Device		Package	DC characterization	CV characterization	AC characterization	Ruggedeness	Temp
Engineering support (Characterization)	Silicon	Diode	Discrete, Module[1)]	VR,IR,VF	C, Total capacitance	Cj,Reverse recovery	UIS, Diode dv/dt	-55c ~ 200°C
		MOSFET		BV,Ids,Rds(on),Igs,Vth,Vsd	Cgd, Cgs, Cds, Ciss, Coss, Crss	Swiching time, Reverse recovery of body diode, Qg	UIS, MOSFET&Diode dv/dt	
		IGBT		BV,Ice,Vce(sat),Ige,Vth,VF	Cies, Coes, Cres, Cgc, Cge, Cce	Switching loss, Swiching time, Reverse recovery of co-pack diode, Qg	SCWT, Latch testing	
	Silicon carbide	Diode		VR,IR,VF	C, Total capacitance	Cj,Qc,Ec	UIS, Diode dv/dt	
		MOSFET		BV,Ids,Rds(on),Igs,Vth,Vsd	Cgd, Cgs, Cds, Ciss, Coss, Crss	Swiching time, Reverse recovery of body diode	UIS, MOSFET&Diode dv/dt, SCWT	
	Gallium Nitride	HEMT		BV,Ids,Rds(on),Igs,Vth	Cgd, Cgs, Cds, Ciss, Coss, Crss	Swiching time, Switching loss, Qg	Dynamic Ron	

1) Depending on the module circuit, need to use each fixtures for testing (Pomme can handle it however, should discuss it in advance)

2) Each equipment should consider how to configure handler, especially ac characteristic should be careful to design handler as minimize parasitic components